High Side Current Monitor 8.0 to 450V, Gain of 5

Features

- Supply voltage 8.0 to 450V
- Voltage output device
- ► Typical gain 5.0±1%
- Max V_{SENSE} 500mV
- Fast rise and fall times, 700ns to 2.0μs
- Maximum quiescent current 50µA

Applications

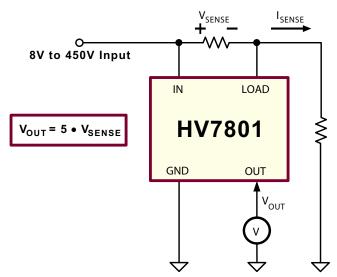
- SMPS current monitor
- ▶ Battery current monitor
- Motor control

General Description

The HV7801 high side current monitor IC transfers a highside current measurement voltage to its ground referenced output with a voltage gain of five. The measurement voltage typically originates at a current sense resistor which is located in a "high side" circuit, such as the positive supply line.

This monitor IC features a very wide input voltage range, high accuracy of transfer ratio, small size, low component count, low power consumption, ease of use, and low cost. Offline applications, battery, and portable applications can be served equally well due to the wide input voltage range and the low quiescent current.

Typical Application Circuit



Ordering Information

Dovice	Package Option
Device	5-Lead SOT-23
HV7801	HV7801K1-G

-G indicates package is RoHS compliant ('Green')





Absolute Maximum Ratings

Parameter	Value
V_{IN}, V_{LOAD}	-0.5V to +450V
V _{OUT}	-0.5V to +10V
V _{SENSE}	-0.5V to +5.0V
Load	±10mA
Operating ambient temperature	-40°C to +85°C
Operating junction temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

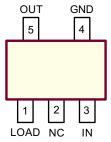
Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Thermal Resistance

Package	$oldsymbol{ heta}_{j_{oldsymbol{a}}}$
5-Lead SOT-23	191 °C/W

Note: Thermal testboard per JEDEC JESD51-7

Pin Configuration



5-Lead SOT-23 (top view)

Product Marking



Y = Last Digit of Year Sealed W = Code for Week Sealed ——— = "Green" Packaging

5-Lead SOT-23

Electrical Characteristics ($T_A = 25$ °C unless otherwise specified, $V_{IN} = 8.0$ to 450V)

Sym	Parameter	Min	Тур	Max	Units	Co	onditions
Supply							
V _{IN}	Supply voltage	8.0	-	450	V	*	
I _Q	Quiescent supply current	-	-	50	μA	-	V _{IN} = 8V to 450V, V _{SENSE} = 0mV
Innut an	d Output	<u> </u>					

Input and Output

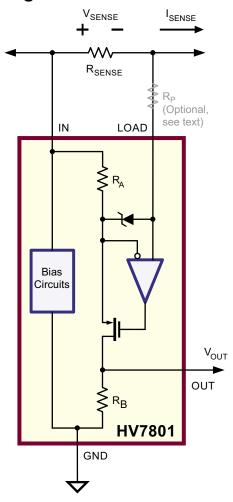
R _{out}	OUT pin output resistance	-	16.5	-	kΩ	-	
V		0	-	65	mV		V _{SENSE} = 0mV
	Output voltage	420	-	580			V _{SENSE} = 100mV
V _{OUT}		913	-	1087		-	V _{SENSE} = 200mV
		2395	_	2605			V _{SENSE} = 500mV

Dynamic Characteristics

4	Output rise time, 10% to 90%	-	0.7	-			V _{SENSE} step 5.0mV to 500mV
RISE		-	-	2.0	μs	-	V _{SENSE} step 0mV to 500mV
t _{FALL}	Output fall time, 90% to 10%	-	0.7	2.0	μs	-	V _{SENSE} step 500mV to 0mV

^{*} Values apply over the full temperature range.

Block Diagram



Application Information

General

The HV7801 high side current monitor IC features accurate current sensing, small size, low component count, low power consumption, exceptional input voltage range, ease of use and low cost.

Typical use is measurement of line or load current for purpose of overcurrent protection, metering and current regulation.

High side current sensing, as opposed to ground referenced or low side current sensing, is desirable or required when:

- ► The current to be measured does not flow in a circuit associated with ground.
- The measurement at ground level can lead to ambiguity due to changes in the grounding arrangement during field use.
- ▶ Introduction of a sense resistor in the system ground is undesirable due to issues with safety, EMI, or signal degradation due to common impedance coupling.

Principle of Operation

The operational amplifier and MOSFET forces the voltage across $\rm R_{\rm A}$ to track $\rm V_{\rm SENSE}$ within the limit of the offset voltage of the opamp, i.e. $\rm V_{\rm RA} = \rm V_{\rm SENSE}.$

The current through $R_{\rm A}$ returns to ground through $R_{\rm B}$. $R_{\rm A}$ and $R_{\rm B}$ are integrated, exhibiting tight matching and excellent tracking. By design, $R_{\rm B}$ is five times larger than $R_{\rm A}$. Consequently, $V_{\rm RB}$ is five times larger than $V_{\rm RA}$, thus resulting in a voltage gain of 5.

OUT Pin Loading Effects

Note that the OUT pin has an typical output resistance of $16.5k\Omega$. Loading the output causes the voltage gain to drop and rise/fall times to increase.

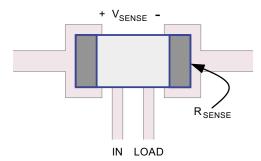
For example, assuming output resistance is $16.5k\Omega$, the load resistance should exceed $16.5M\Omega$ in order to limit the drop in gain to 1 part in 1000.

Again assuming output resistance is $16.5k\Omega$, capacitive loading of 6pF results in a response pole with a time constant of 100ns, not high enough to materially affect the output rise and fall times (about 700ns).

Sense Resistor Considerations

Limit the sense resistor voltage to 500mV during normal operating conditions. Limit the power dissipation in the sense resistor to suit the application; a high sense voltage benefits accuracy, but increases power dissipation.

Consider the use of Kelvin connections for applications where considerable voltage drops may occur in the PCB traces. A layout pattern which minimizes voltage across the sense lines is shown below.



Choose a low inductance type sense resistor if preservation of bandwidth is important. The use of Kelvin connections helps by excluding the inductive voltage drop across the traces leading to the sense resistor. The inductive voltage drop may be substantial when operating at high frequencies. A trace or component inductance of just 10nH contributes an impedance of $6.2 \text{m}\Omega$ at 100 kHz, which constitutes a 6% error when using a $100 \text{m}\Omega$ sense resistor.

Transient Protection

Add a protection resistor (R_p) in series with the LOAD pin if V_{SENSE} can exceed 5V in a positive sense or 600mV in a negative sense, whether in a steady state or in transient conditions.

A large V_{SENSE} may occur during system startup or shutdown due to the charging and discharging of bulk storage capacitors. V_{SENSE} may be large due to fault conditions, such as a short circuit condition, or a broken or missing sense resistor.

An internal 5V Zener diode with a current rating of 10mA protects the sense amplifier inputs. The block diagram shows the orientation of this diode. The Zener diode provides clamping at 5V for a positive $V_{\rm SENSE}$ and at 600mV for a negative $V_{\rm SENSE}$.

Under worst case conditions, limit the Zener current to 10mA. A 100k Ω resistor limits the maximum Zener diode current to 4.5mA when V_{SENSE} is 450V, whether positive or negative. Note that the protection resistor may affect the bandwidth. The resistor forms an RC network with the trace and pin capacitance at the LOAD pin. A capacitance of 5pF results in a time constant of 500ns.

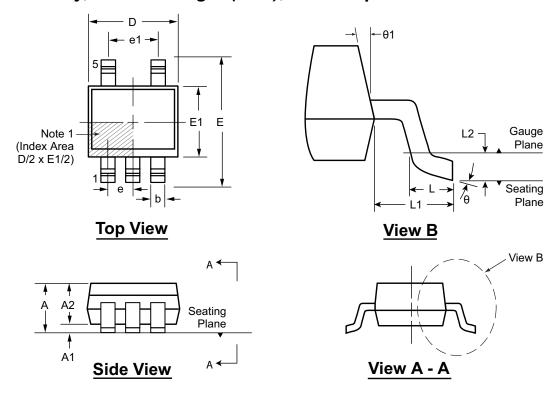
The protection resistor may cause an offset voltage due to bias current at the LOAD input. Under worst case bias current (1nA), a $100k\Omega$ protection resistor could cause an offset of $100\mu V$ or 0.2% of full scale. Note that the bias current is nominally zero as the LOAD is a high impedance CMOS input.

Pin Description

Pin#	Pin Name	Description
1	LOAD	Sense amplifier input. High impedance input with Zener diode protection. Add an external protection resistor in series with LOAD if V _{SENSE} exceeds the range of -600mV to +5V.
2	NC	No connect. This pin must be left floating for proper operation.
3	IN	Sense amplifier input and supply.
4	GND	Supply return.
5	OUT	Output with a nominal output resistance of $16.5k\Omega$. Preservation of accuracy may require an external buffer amplifier to prevent excessive loading.

5-Lead SOT-23 Package Outline (K1)

2.90x1.60mm body, 1.45mm height (max), 0.95mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	ol	Α	A1	A2	b	D	E	E1	е	e1	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.90*	0.00	0.90	0.30	2.75*	2.60*	1.45*	0.95 BSC	1.90 BSC 0	0.30	0.60 REF	0.25 BSC	0 o	5°
	NOM	-	-	1.15	-	2.90	2.80	1.60			0.45			4 °	10°
	MAX	1.45	0.15	1.30	0.50	3.05*	3.00*	1.75*			0.60	_	D00	8 º	15°

JEDEC Registration MO-178, Variation AA, Issue C, Feb. 2000.

Drawings not to scale.

Supertex Doc. #: DSPD-5SOT23K1, Version NR110308.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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^{*} This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.