High Speed ±100V 2A Integrated Ultrasound Pulser

Features

- HVCMOS technology for high performance
- 0 to ±100V output voltage
- ±2.0A source and sink current
- Built-in damping for RTZ waveform capability
- Gate-clamp for quick output amplitude ramping
- Up to 40MHz operation frequency
- ±3ns matched delay times
- Second harmonic is less than -40dB
- 1.8 to 3.3V CMOS logic interface
- 7x7 thermally-enhanced 44-lead QFN MCM

Application

- Medical ultrasound imaging

General Description

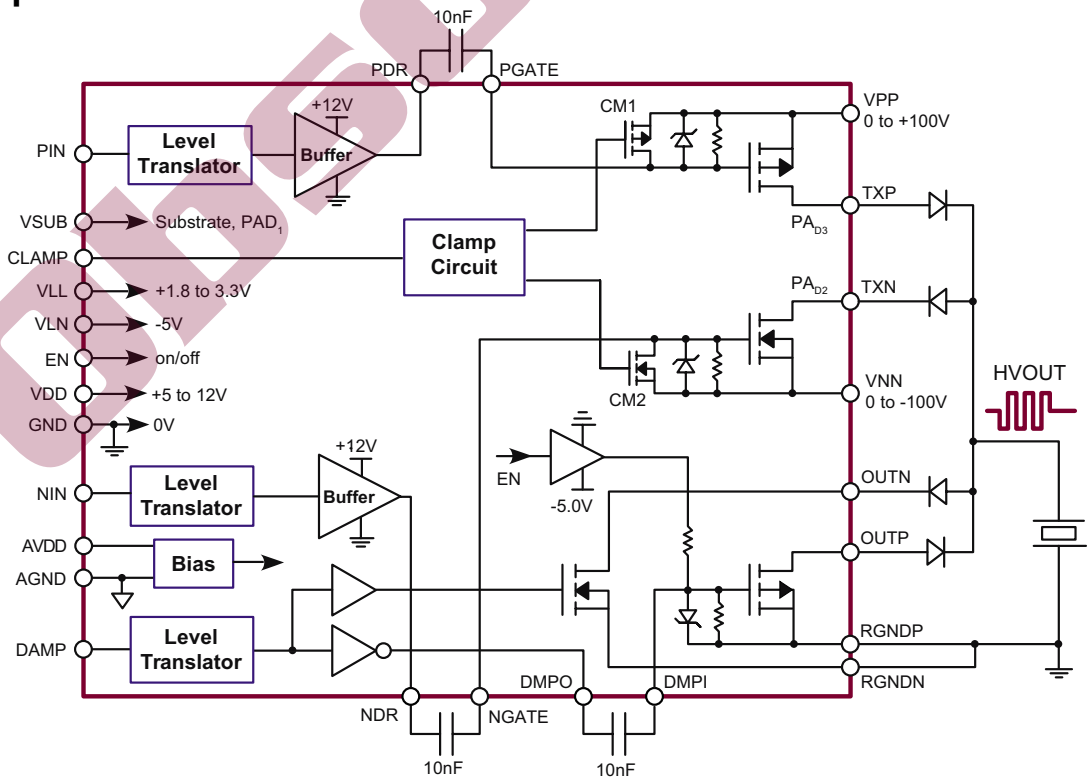
The Supertex HV732 is a single, complete, high-voltage, high-speed, ultrasound transmitter pulser. It is designed for medical ultrasound imaging applications.

The HV732 consists of a control logic circuit, level translators, MOSFET gate drive buffers, clamp circuits, and high current, high voltage MOSFETs as the ultrasound transmitter pulser output stage. The output stage also has damping transistors which allows a faster return-to-zero (RTZ) waveform. For applications which require the high voltage supplies, V_{PP} and V_{NN}, to change rapidly (faster than 10nF x 10kΩ), a clamp pin is provided. This keeps the high voltage output transistors 'off' during the rapid change in supply voltage.

In the output stage there are two pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance, and can provide peak currents of over ±2.0 amps. The built-in MOSFET gate driver outputs swing 0 to 12V on PDR and NDR pins. The P-channel damp output swings 0 to 12V on the DMPO pin.

Obsolete

Typical Application Circuit

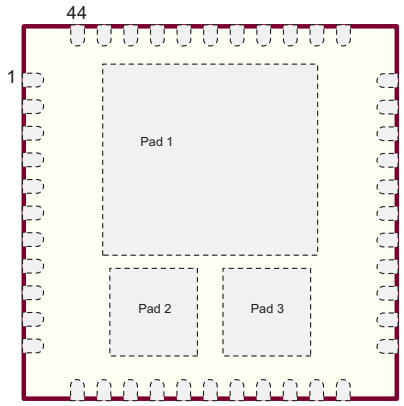


Ordering Information

Device	44-Lead QFN *7.00x7.00mm body* *1.00mm height (max)* *0.50mm pitch, 3 pads*
HV732	HV732K6-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



44-Lead QFN (K6)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{LL}, logic supply	-0.5V to +5.5V
V_{DD}, positive gate drive supply	-0.5V to +15V
AV_{DD}, positive gate drive supply	-0.5V to +15V
V_{LN}, negative gate drive supply	-5.5V to +0.5V
V_{PP}-V_{NN}, differential high voltage supply	+220V
V_{PP}, high voltage positive supply	-0.5V to +200V
V_{NN}, high voltage negative supply	+0.5V to -200V
Storage temperature	-65°C to 150°C
Thermal enhanced package power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or

44-Lead QFN (K6)

Operating Supply Voltages and Current

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD}$ = 12V, V_{LL} = 3.3V, V_{LN} = -5.0V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Logic supply	1.8	3.3	3.6	V	---
AV_{DD}	Positive analog supply	9.0	-	12.6	V	---
V_{DD}	Positive drive supply	9.0	-	12.6	V	---
V_{PP}	High voltage positive supply	0	-	100	V	---
V_{NN}	High voltage negative supply	-100	-	0	V	---
V_{LN}	Negative supply	-4.75	-5.0	-5.25	V	---
V_{SUB}	High voltage positive supply for to bias substrate	-	-	100	V	Need to be the most positive supply on the device
I_{DDQ}	V_{DD} current EN = Low	-	175	290	µA	All other inputs Low.
I_{DDEN}	V_{DD} current EN = High	-	1.7	2.8	mA	All other inputs Low.
I_{DDEN}	V_{DD} current at 5MHz PW	-	7.5	-	mA	f = 5.0MHz, PW D% = 1.0, No cap on P_{DR}, N_{DR}
I_{PPQ}	V_{PP} current EN = Low	-	2.0	5.0	µA	V_{PP} = +100V, V_{NN} = -100V, All other inputs Low.
I_{PPEN}	V_{PP} current EN = High	-	140	180	µA	V_{PP} = +100V, V_{NN} = -100V, All other inputs Low.
I_{NNQ}	V_{NN} current EN = Low	-	-1.0	-3.0	µA	V_{PP} = +100V, V_{NN} = -100V, All other inputs Low.

Obsolete

Operating Supply Voltages and Current (cont.)

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5.0V$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{NNEN}	V_{NN} current EN = High	-	-140	-180	µA	V_{PP} = +100V, V_{NN} = -100V, , All other inputs Low.
I_{LLQ}	V_{LL} current EN = Low	-	1.0	5.0	µA	All other inputs Low.
I_{LLEN}	V_{LL} current EN = High	-	16	25	µA	All other inputs Low.
I_{LNQ}	V_{LN} current EN = Low	-	-1.0	-5.0	µA	All other inputs Low.
I_{LNEN}	V_{LN} current EN = High	-	-230	-320	µA	All other inputs Low.

DC Electrical Characteristics

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5.0V$, $T_A = 25°C$)

Output P-Channel MOSFET, TX_P

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-2.0	-	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance	-	-	8.0	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	10	-	50	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	-13.2	-	-25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	-0.5	-	-0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	25	55	pF	

Output N-Channel MOSFET, TX_N

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	2.0	-	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance		-	7.0	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	10	-	50	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	13.2	-	25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	0.5	-	0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.0	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	28	60	pF	

Output P-Channel Damp MOSFET, OUT_P

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	-1.0	-	A	V_{GS} = -10V, V_{DS} = -25V
R_{ON}	Channel resistance	-	-	30	Ω	V_{GS} = -10V, I_{DS} = -1.0A
R_{GS}	Gate to source resistor	-	75	100	KΩ	I_{GS} = -100µA
V_{GS}	Source to gate zener voltage	-13.2	-	-25	V	I_{GS} = -2.0µA
V_{GSF}	Gate zener forward voltage	0.5	-	0.8	V	---
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.6	V	I_{DS} = -1.0mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1Mhz
C_{OSS}	Output capacitance	-	-	60	pF	

Obsolete

Output N-Channel Damp MOSFET, OUT_N

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	1.0	-	A	V_{GS} = 10V, V_{DS} = 25V
R_{ON}	Channel resistance	-	-	22	Ω	V_{GS} = 10V, I_{DS} = 0.5A
V_{GS}	Source to gate zener voltage	1.0	-	2.6	V	I_{DS} = 1.0µA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1Mhz
C_{OSS}	Output capacitance	-	-	60	pF	

P-Channel Gate Driver Output, P_{DR}

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	10	15	Ω	I_{PDR} = 100mA
R_{SOURCE}	Output source resistance	-	8.0	13	Ω	I_{PDR} = -100mA
I_{PDR}	Peak output sink current	-	2.0	-	A	---
I_{PDR}	Peak output source current	-	-2.0	-	A	---

N-Channel Gate Driver Output, N_{DR}

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	8.0	13	Ω	I_{NDR} = 100mA
R_{SOURCE}	Output source resistance	-	9.0	14	Ω	I_{NDR} = -100mA
I_{NDR}	Peak output sink current	-	1.0	-	A	---
I_{NDR}	Peak output source current	-	-1.0	-	A	---

P-Channel Gate Driver Output, DMPO

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	36	45	Ω	I_{DMPO} = 100mA
R_{SOURCE}	Output source resistance	-	36	45	Ω	I_{DMPO} = -100mA
I_{DMPO}	Peak output sink current	-	0.3	-	A	---
I_{DMPO}	Peak output source current	-	-0.3	-	A	---

P-Channel Gate Clamp MOSFET

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	100	-	mA	---
R_{ON}	Channel resistance	-	60	80	Ω	---
C_{OSS}	Output capacitance	-	40	-	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0Mhz

N-Channel Gate Clamp MOSFET

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{OUT}	Output saturation current	-	50	-	mA	---
R_{ON}	Channel resistance	-	25	50	Ω	---
C_{OSS}	Output capacitance	-	40	-	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0Mhz

Obsolete

Logic Inputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Inputs rise and fall time	-	-	10	ns	Logic input edge speed requirement
V_{IH}	Input logic high voltage	$0.8V_{LL}$	-	V_{LL}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{LL}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---

AC Electrical Characteristics

(Over recommended operating conditions unless otherwise specified: $AV_{DD} = V_{DD} = 12V$, $V_{LL} = 3.3V$, $V_{LN} = -5.0V$, $T_A = 25°C$)

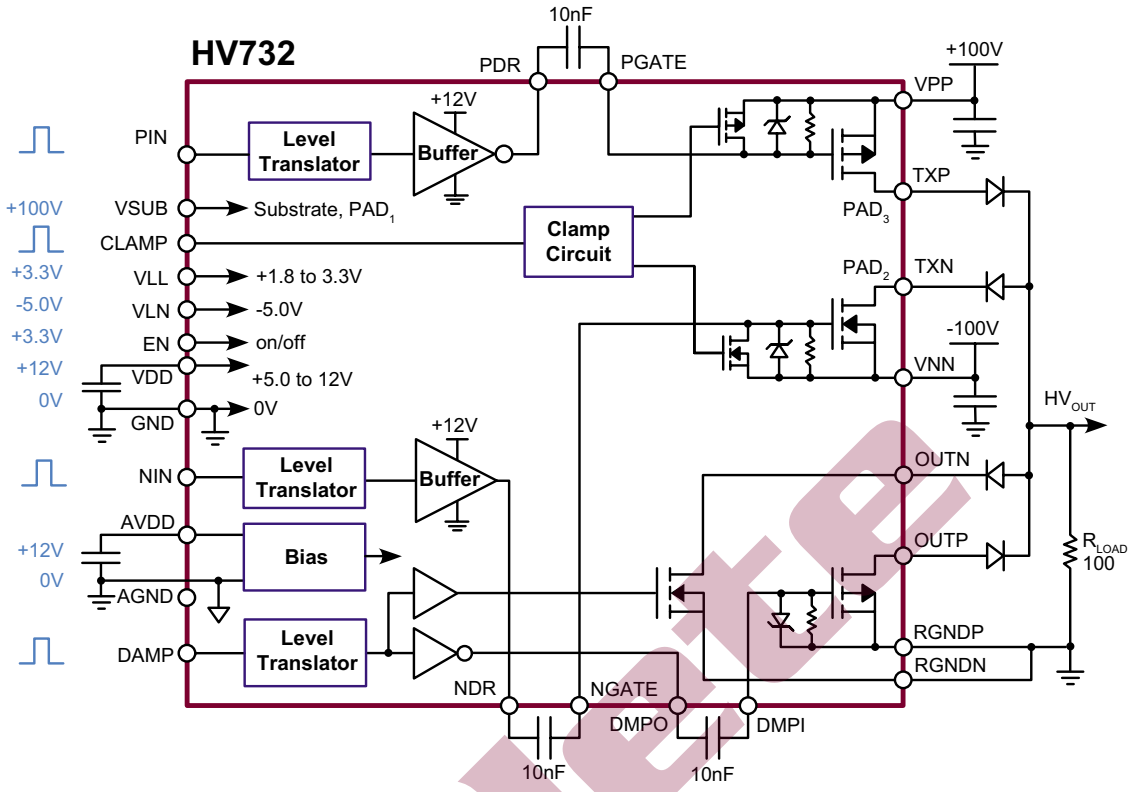
Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{out}	Output frequency range	-	-	40	MHz	See test curcuit and timing diagram
t_r	Output rise time	-	10	-	ns	See relevant test circuit and timing diagram. Load = 1.0kΩ/220pF
t_f	Output fall time	-	10	-	ns	
t_{dr}	Delay time on rise time	14	-	22	ns	
t_{df}	Delay time on fall time	14	-	22	ns	
Δt_{delay}	Delay time matching	-	±3.0	-	ns	From device to device
HD2	Second harmonic distortion	-	-40	-	dB	100Ω resistor load
t_{jitter}	Output jitter	-	80	-	ps	Standard deviation of t_d samples (1.0k)
t_{EN}	Enable time	-	30	50	µs	See timing diagram
$t_{DMPON(P)}$	Damp switch on delay (P)	-	17	22	ns	OUTP 50Ω to -15V, 10nF from DMPO to DMPI. See timing diagram.
$t_{DMPOFF(P)}$	Damp switch off delay (P)	-	20	26	ns	
$t_{DMPON(N)}$	Damp switch on delay (N)	-	13	17	ns	OUTN 50Ω to +15V. See timing diagram.
$t_{DMPOFF(N)}$	Damp switch off delay (N)	-	13	17	ns	
$t_{CLPON(P)}$	Clamp switch on delay (P)	-	430	1000	ns	P_{GATE} 75Ω to 0V, 10nF to P_{DR}, V_{PP} = +12V. See timing diagram.
$t_{CLPOFF(P)}$	Clamp switch off delay (P)	-	490	1000	ns	
$t_{CLPON(N)}$	Clamp switch on delay (N)	-	330	550	ns	N_{GATE} 75Ω to 0V, 10nF to N_{DR}, V_{NN} = -12V. See timing diagram.
$t_{CLPOFF(N)}$	Clamp switch off delay (N)	-	316	500	ns	
t_{PWRUP}	Device power-up delay	-	150	200	µs	All power supplies up and stable

Power-Up Sequence	
1	V_{SUB}
2	V_{PP}
3	V_{NN} and V_{LN}
4	V_{DD} and V_{LL}
5	EN = High
6	Other inputs active

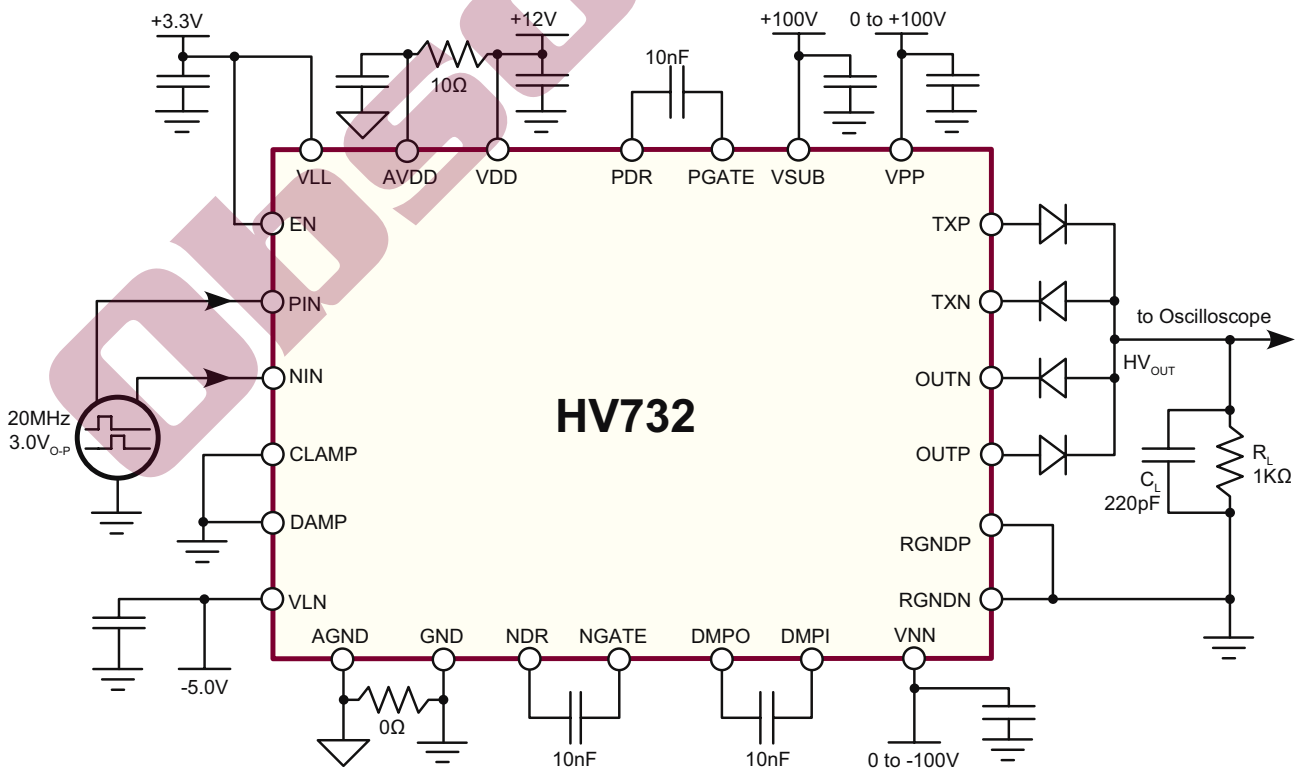
Power-Down Sequence	
1	Other inputs inactive
2	EN = Low
3	V_{DD} and V_{LL}
4	V_{NN} and V_{LN}
5	V_{PP}
6	V_{SUB}

Obsolete

HV732 Test Circuit



HV732 TX Switching Time Test



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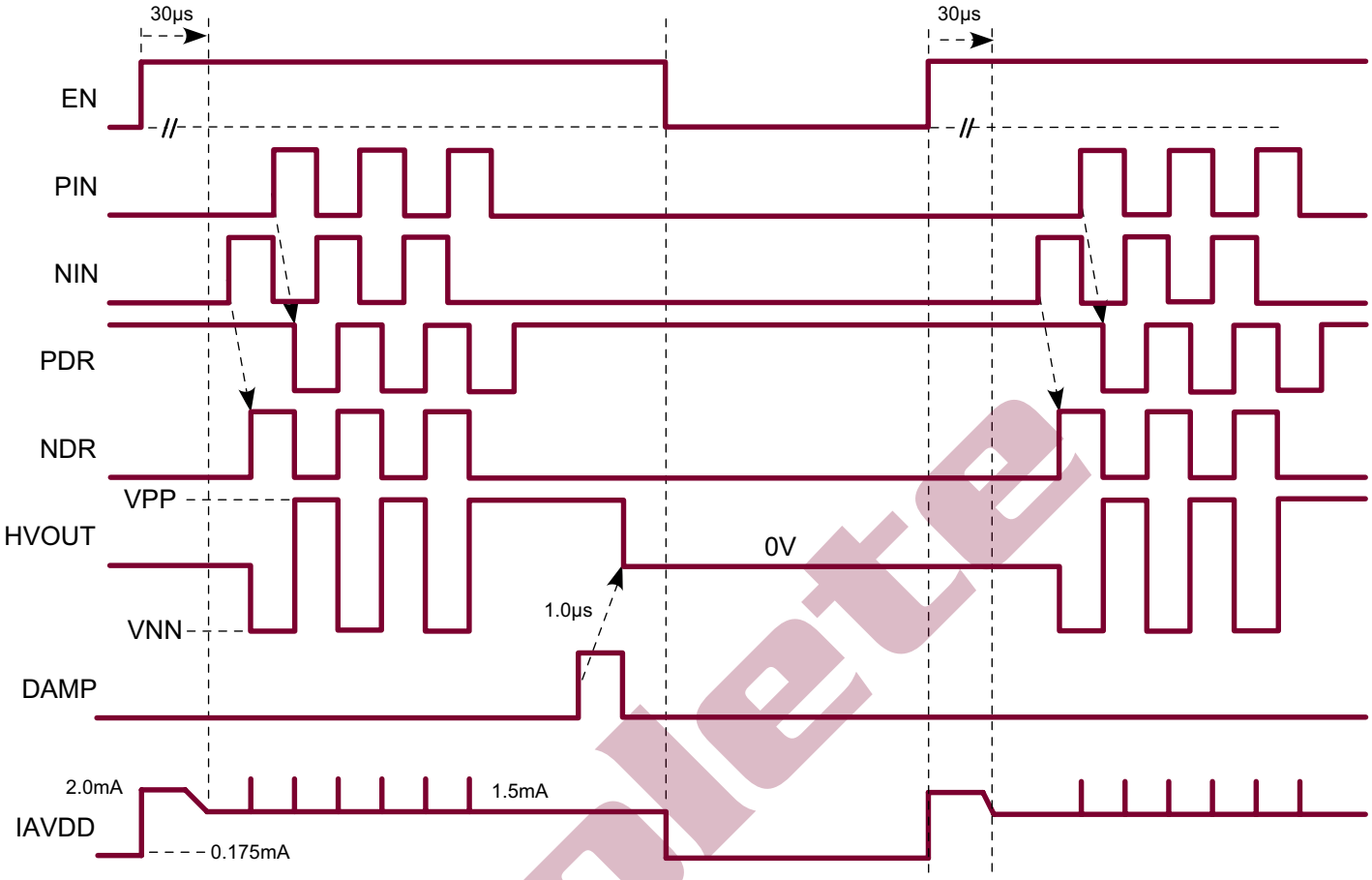
HV732 Timing Diagram

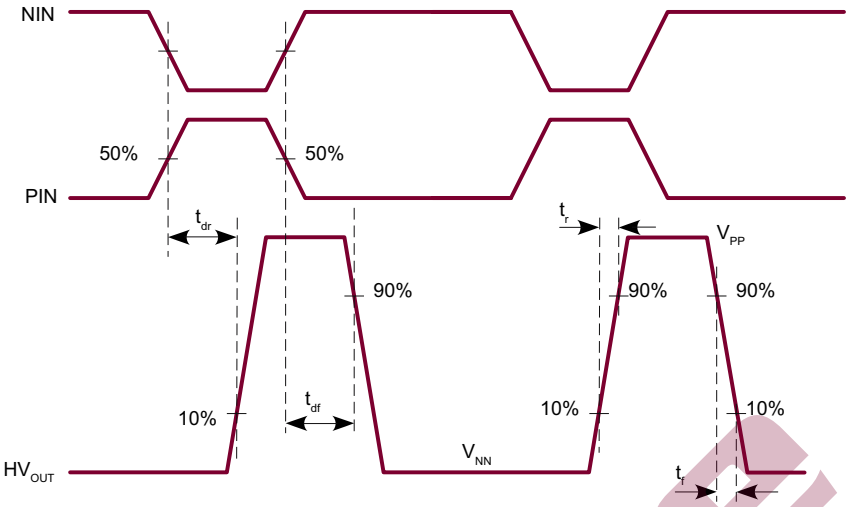


Truth Table

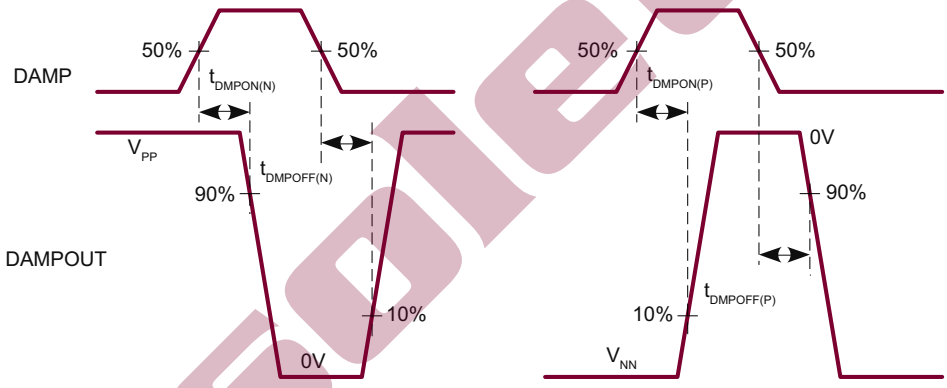
Logic Control Inputs					Gate Drive Output			HV Output		Damp Output		Clamp	
EN	P_{IN}	N_{IN}	CLAMP	DAMP	P_{DR}	N_{DR}	DMPO	TX_P	TX_N	OUT_P	OUT_N	CM1	CM2
1	0	0	0	0	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF
1	**1**	0	0	0	**L**	L	H	**ON**	OFF	OFF	OFF	OFF	OFF
1	0	**1**	0	0	H	**H**	H	OFF	**ON**	OFF	OFF	OFF	OFF
1	**X**	**X**	**1**	0	H	L	H	OFF	OFF	OFF	OFF	ON	ON
1	0	0	0	**1**	H	L	**L**	OFF	OFF	**ON**	**ON**	OFF	OFF
0	X	X	X	X	H	L	**L**	OFF	OFF	**ON**	**ON**	ON or OFF	ON or OFF

Obsolete

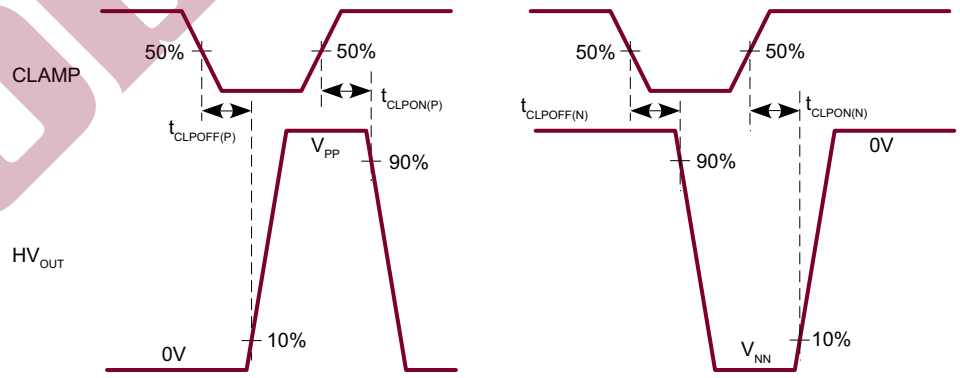
HV732 TX Switching Time Diagram



HV732 DAMP Switching Time Diagram



HV732 Clamp Switching Time Diagram



Obsolete

Pin Description

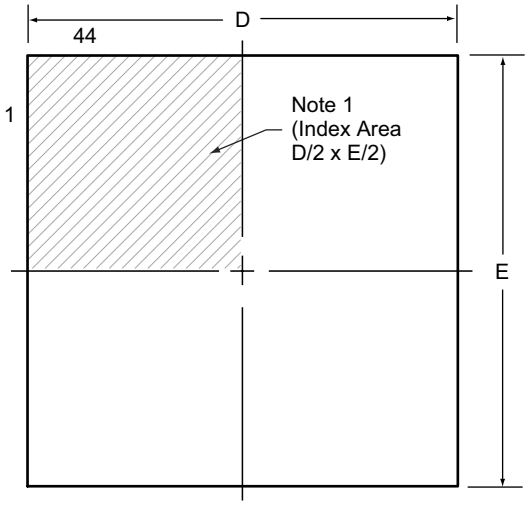
Pin	Function	Description
1	DMPO	Output of low voltage drive buffer for P-channel damp, 10nF external cap to pin 34 (DMPI)
2	GND	Drive power ground
3	NDR	Output of low voltage drive buffer for N-DMOS, 10nF external cap to pin 9 (NGATE)
4, 5	VDD	Positive voltage supply for drive circuitry (+12V)
6	VSUB	Substrate connection of control / driver die chip (connected to the most positive supply, VPP)
7	RGNDN	Ground return of damp N-DMOS source
8	OUTN	Output of damp N-DMOS drain (open drain output)
9	NGATE	Gate input of the high voltage N-DMOS, 10nF external cap from pin 3 (NDR)
10, 11, 12, 13, 14	VNN	Negative high voltage power supply (-100V)
15, 16	TXN	Output of the high voltage N-DMOS drain (open drain output)
17	NC	No connection
18, 19	TXP	Output of the high voltage P-DMOS drain (open drain output)
20, 21, 22, 23, 24	VPP	Positive high voltage power supply (+100V)
25	PGATE	Gate input of the high voltage P-DMOS, 10nF external cap from pin 31 (PDR)
26	OUTP	Damp P-DMOS drain (open drain output)
27	RGNDP	Ground return of damp P-DMOS
28	VSUB	Substrate connection of control / driver die chip (connected to the most positive supply, VPP)
29, 30	VDD	Positive voltage supply for drive circuitry (+12V)
31	PDR	Output of low voltage drive buffer for P-DMOS, 10nF external cap to pin 25 (PGATE)
32, 33	GND	Drive power ground
34	DMPI	Connects to damp power P-DMOS gate, 10nF cap to pin 1 (DMPO)
35	PIN	Input logic control of the high voltage P-DMOS pin 18 &19 (TXP), High = on, Low = off
36	VLN	Negative low voltage power supply (-5.0V)
37	AVDD	Positive analog voltage power supply (+12V)
38	AGND	Analog signal ground (0V)
39	VSUB	Substrate connection of control / driver chip (connected to the most positive supply)
40	EN	Control / drive chip power enable High = on, Low = off. When EN = Low both damping outputs, OUTN and OUTP, will be on.
41	DAMP	Input of damp control on both pin 26 (OUTP) and pin 8 (OUTN), Hi = on, Low = off
42	CLAMP	Input of clamp switches on both gates of output P-DMOS and N-DMOS, High = on, Low = off (EN = High)
43	VLL	Positive voltage supply of low voltage logic (+1.8V to +5V)
44	NIN	Input logic control of the high voltage N-DMOS pin 15 & 16 (TXN), High = on, Low = off

Note:
The three thermal slabs on the bottom of the package must be externally connected PAD1 to VSUB, PAD2 to TXN, and PAD3 to TXP.

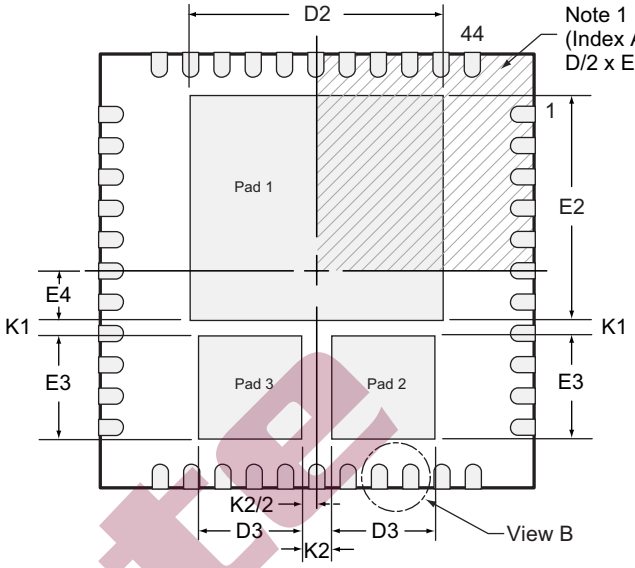
Obsolete

44-Lead QFN Package Outline (K6)

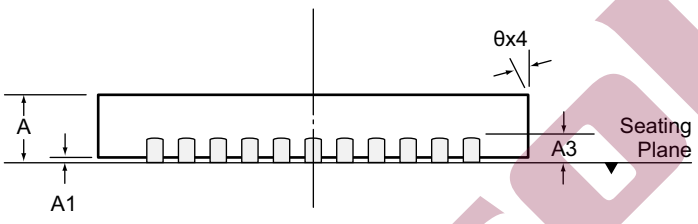
7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch, 3 pads



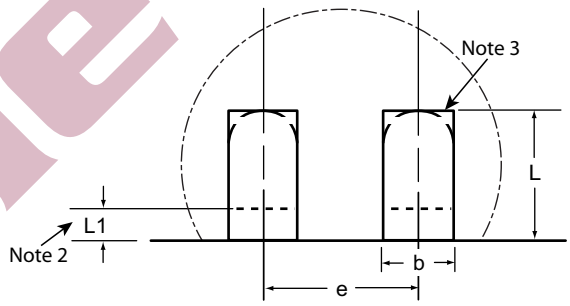
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	D3	E	E2	E3	E4	e	K1	K2	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	6.85	4.20	1.57	6.85	3.20	1.75	0.53	0.50 BSC	0.30	0.41	0.35	0.00	0
	NOM	0.90	0.02		0.25	7.00	4.30	1.67	7.00	3.30	1.85	0.55		0.35	0.46	0.40	-	-
	MAX	1.00	0.05		0.30	7.15	4.40	1.77	7.15	3.40	1.95	0.58		0.40	0.51	0.45	0.15	14

Drawings not to scale.
Supertex Doc. #: *DSPD-44QFNK67X7P050, Version B101008.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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