4-Channel Low-Noise Amplifier

Features

- 2.5 ± 0.125V operation
- 4 independent channels
- Fully differential inputs and outputs
- 0.74nV/√Hz input-referred noise at 18.5dB gain
- Ultra low current noise 0.35pA /√Hz
- 600kΩ /17.5pF internal input impedance
- 100MHz amplifier bandwidth
- Linear-in-dB continuous variable gain control
- Four digital programmable gain settings for PGA
- 60MHz whole channel bandwidth at maximum gain
- 70dB maximum channel gain
- Variable gain scaling control
- Active input impedance matching

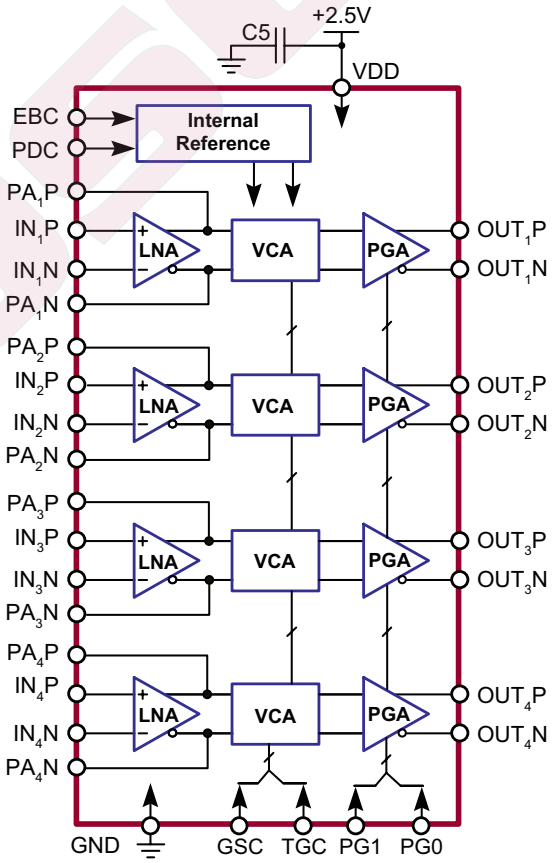
Applications

- Medical ultrasound receiver LNA & TGC
- Doppler signal amplification
- Transducer signal conditioning

General Description

The MD3880 is a 4-channel, variable gain amplifier (VGA) paired with a low noise amplifier (LNA) that delivers fully differential input and output for ultrasound applications. The 18.5dB gain of the LNA allows the whole channel to have 0.74nV/√Hz of input-referred voltage noise at 5MHz. The LNA is capable of active impedance control to improve noise performance, provided that the applications can take advantage of input impedance matching. The output of the LNA is fed directly into the VGA without using an external coupling capacitor. The VGA is composed of a voltage controlled attenuator (VCA) and a programmable gain amplifier (PGA). The VCA can be continuously varied linear-in-dB by a control voltage (V_{TGC}) from 0dB to a maximum 47dB. In addition, the gain of the PGA can be varied between four discrete settings.

Typical Application Circuit

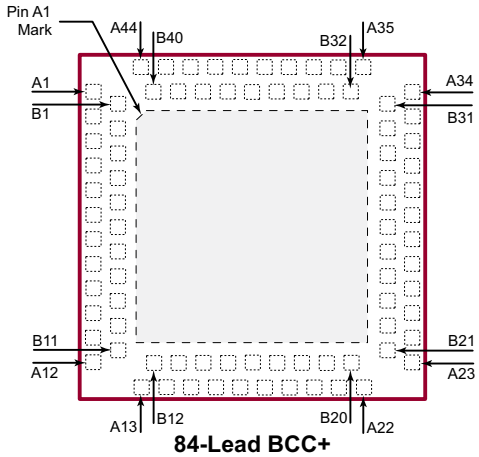


Ordering Information

Device	Package Option
	84-Lead BCC+ *7.00x7.00mm body* *0.80mm height (max)* *0.50mm pitch*
MD3880	MD3880B2-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



84-Lead BCC+
(Top View)

Absolute Maximum Ratings

Parameter	Value
V_{DD}, positive supply	-0.5V to +3.5V
V_{IN}, any input pin voltage range	-0.5V to V_{DD}
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C
Power dissipation	2.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
___ = "Green" Packaging

Package may or may not include the following marks: Si or

84-Lead BCC+ Package

Operating Supply Voltages

(Over operating conditions unless otherwise specified, V_{DD} = +2.5V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power supply	2.375	2.5	2.625	V	T_A = -40°C to +85°C
I_{DDQ}	V_{DD} supply current	-	-	45	mA	Power down, PDC=1, total of all channels
I_{DD}	V_{DD} supply current	-	75	-	mA	PDC = 0
PWR	Power dissipation	-	700	-	mW	Total of all channels
		-	175	-	mW	Per channel
PSRR	PSRR	-	-60	-	dB	f = 100kHz

Logic Data and Clock Inputs Characteristics

(Over operating conditions unless otherwise specified, V_{DD} = +2.5V, T_A = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input logic high voltage	$0.8V_{DD}$	-	V_{DD}	V	---
V_{IL}	Input logic low voltage	0	-	$0.2V_{DD}$	V	---
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---
C_{IN}	Input logic pin capacitance	-	10	-	pF	---

Electrical Characteristics

(All typical values are under the condition of T_A= + 25°C, V_{DD} = 2.5V, Load resistance = 1.0kΩ across the differential outputs, C_{LOAD} = 1.0pF, f_{IN} = 10MHz, PG0 = 0, PG1 = 0, V_{GSC} = 2.5V, V_{CM} = 1.25V, $GAIN_{LNA}$ = 18.5dB, Single-ended input: R_S = R_{IN} = 50Ω. R_{IN} is formed by active termination with R_{FB} = 237Ω and C_{FB}, Differential signal output, unless otherwise noted.)

Low Noise Amplifier

Sym	Parameter	Min	Typ	Max	Units	Conditions
G_{LNA}	Amplifier gain	-	18.5	-	dB	---
R_{IN}	Input resistance	-	600	-	kΩ	Without active termination
C_{IN}	Input capacitance	-	17.5	-	pF	Without active termination
I_{BIAS}	Input bias current	-	1.0	-	nA	From ESD leakage
CMRR	Common mode rejection ratio	-	-65	-	dB	PG0 = PG1 = V_{DD}, V_{TGC} = 2.0V, f = 1.0MHz
V_{IN}	Input voltage range	-	±210	-	mV	AC-coupled
$V_{IN\text{-}NOISE}$	Input voltage noise, 5MHz	-	0.74	-	nV/√Hz	Without active termination
$I_{IN\text{-}NOISE}$	Input current noise	-	0.35	-	pA/√Hz	Without active termination
NF	Noise figure	-	2.3	-	dB	f = 5.0MHz, without active termination
		-	3.7	-	dB	R_S = R_{IN} = 50Ω, f = 5.0MHz with active termination
BW	Bandwidth	-	100	-	MHz	Small signal bandwidth

Overall Channel

Sym	Parameter	Min	Typ	Max	Units	Conditions
Gain	Whole channel gain	-	70	-	dB	Without active termination, max. gain
BW_{VGA}	-3dB bandwidth	-	60	-	MHz	Small signal bandwidth at max. gain
SR_{VGA}	Slew rate	-	500	-	V/µs	---
VO_{VGA}	Output signal range	-	4	-	V_{PP}	RL > 1.0kΩ differentially
R_{OUT}	Output Impedance	-	3.0	-	Ω	f = 5.0MHz, single ended
I_{OUTS}	Output short-circuit current	-	±40	-	mA	---
$V_{IN\text{-}NOISE}$	Input voltage noise	-	0.8	-	nV/√Hz	At max. gain and 5.0MHz
IMD	Intermodulation distortion, two-tone	-	-76	-	dBc	1MHz , V_{OUT} = 1.0V_{PP}, 30dB gain
		-	-70	-		10MHz , V_{OUT} = 1.0V_{PP}, 30dB gain
HD3	Third harmonic distortion	-	-73	-	dBc	V_{OUT} = 1.0V_{PP}, 1.0MHz, 30dB gain
		-	-69	-		V_{OUT} = 1.0V_{PP}, 10MHz, 30dB gain
		-	-55	-		V_{OUT} = 1.0V_{PP}, 1MHz, 10dB gain
		-	-47	-		V_{OUT} = 1.0V_{PP}, 10MHz, 10dB gain
HD2	Second harmonic distortion	-	-87	-	dBc	V_{OUT} = 1.0V_{PP}, 1MHz, 30dB gain
		-	-70	-		V_{OUT} = 1.0V_{PP}, 10MHz, 30dB gain
		-	-53	-		V_{OUT} = 1.0V_{PP}, 1MHz, 10dB gain
		-	-51	-		V_{OUT} = 1.0V_{PP}, 10MHz, 10dB gain
A_{OUT1dB}	1dB compression point	-	-1.3	-	dBm	V_{OUT} = 1.0V_{PP}, f= 10MHz, 8dB gain

Overall Channel

Sym	Parameter	Min	Typ	Max	Units	Conditions
CSTK	Crosstalk	-	-78	-	dB	PG0 and PG1 = 1, 30dB gain, 1.0MHz, 1.0V_{PP} at adjacent channel
Δt_{gd}	Group delay variation	-	±2.0	-	ns	2 MHz < f < 50 MHz, Full Gain Range
t_{OLR}	Overload recovery time	-	5.0	-	ns	8dB Gain, V_{IN} = 50mV_{PP} to 1.0V_{PP} change, f = 10MHz
V_{DC-OUT}	DC output level, V_{IN} = 0	-	1.25	-	V	---

Note: *V_{IN} is the voltage at the non-inverting node of the amplifier.*

Accuracy

Sym	Parameter	Min	Typ	Max	Units	Conditions
G_{SLOPE}	Gain slope	31	33	35	dB/V	V_{GSC} = 2.5V
G_{MAT}	Ch. to ch. gain matching	-	±0.1	-	dB	V_{TGC} = 0V or 2.0V
E_{GAIN}	Gain error	-	±0.8	-	dB	Referenced to best fit dB-linear curve, 0.5V < V_{TGC} < 1.7V
V_{OS-OUT}	Output offset voltage	-	±20	-	mV	Reference to 1.25V

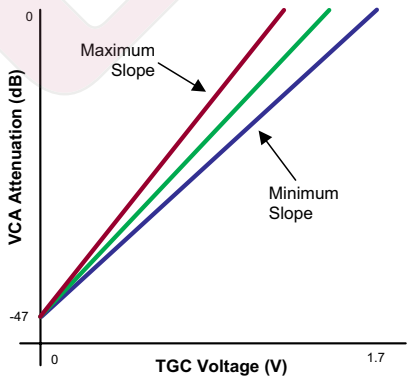
Gain Control Interface

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{TGC}	Gain control voltage	0	-	2	V	Linear in dB, See gain scaling diagram
V_{GSC}	Gain slope voltage	2.0	-	2.5	V	About 41dB/V at 2.0V and 33dB/V at 2.5V
R_{GSC}	Input resistance of GSC	-	120	-	kΩ	---
R_{TGC}	Input resistance of TGC	-	1.5	-	MΩ	Connected to ¾ V_{GSC}
td_{TGC}	Response time	-	0.2	-	µs	95% full gain change

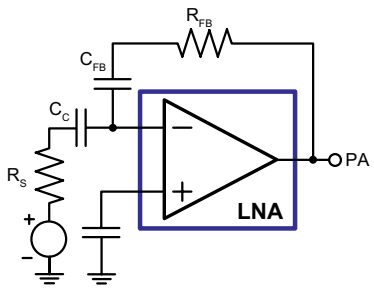
PGA Gain Control Table

PG1, PG0	PGA Gain (dB)
0,0	35
0,1	40.5
1,0	46
1,1	51.5

TGC and GSC Voltage for Gain Scaling



Configurations for Active Feedback



Pin Configuration

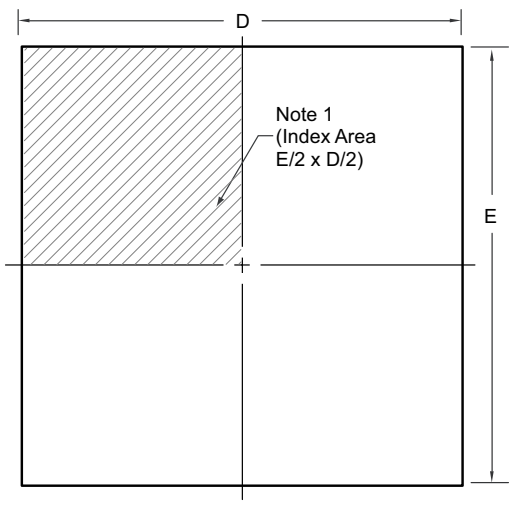
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A1	IN_1P	A22	AGND	A43	GND	B20	NC
A2	IN_1N	A23	AVDD	A44	AGND	B21	OUT_4P
A3	PA_1P	A24	AVDD	B1	PA_1N	B22	CM4
A4	PA_2N	A25	AGND	B2	AVDD	B23	OUT_4N
A5	AVDD	A26	OUT_3P	B3	AGND	B24	AV_{DD}
A6	PA_2P	A27	CM3	B4	IN_2P	B25	AVDD
A7	PA_3N	A28	OUT_3N	B5	IN_2N	B26	AGND
A8	AVDD	A29	OUT_2P	B6	AGND	B27	AVDD
A9	PA_3P	A30	CM2	B7	IN_3P	B28	AVDD
A10	AGND	A31	OUT_2N	B8	IN_3N	B29	AGND
A11	IN_4P	A32	OUT_1P	B9	PA_4N	B30	CM1
A12	IN_4N	A33	AVDD	B10	AVDD	B31	OUT_1N
A13	AGND	A34	AVDD	B11	PA_4P	B32	NC
A14	AGND	A35	AGND	B12	NC	B33	NC
A15	EBC	A36	GND	B13	GND	B34	NC
A16	AGND	A37	VDD	B14	PDC	B35	NC
A17	GSC	A38	VDD	B15	AVDD	B36	NC
A18	CM0	A39	GND	B16	NC	B37	NC
A19	A0	A40	GND	B17	A1	B38	NC
A20	PG1	A41	VDD	B18	PG0	B39	NC
A21	GND	A42	VDD	B19	TGC	B40	NC

Pin Description

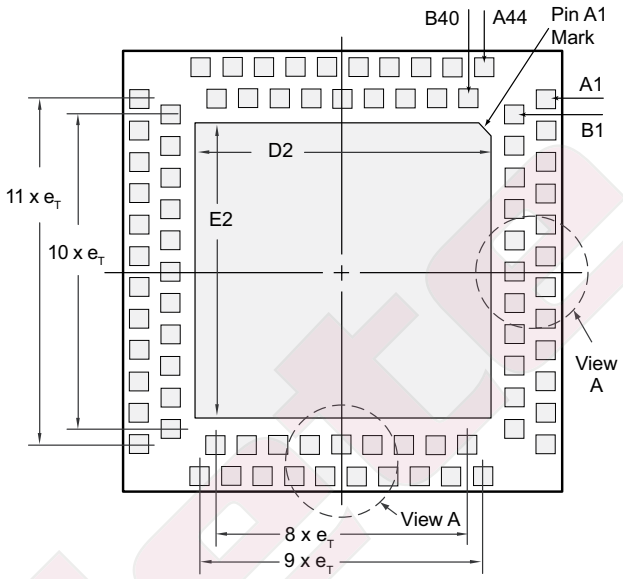
Pin Name	Description
VDD	VDD voltage supply
GND	Ground
AVDD	Analog supply
AGND	Analog ground
$IN_{1\sim4}P$	Positive polarity LNA input of channel 1~4
$IN_{1\sim4}N$	Negative polarity LNA input of channel 1~4
$PA_{1\sim4}P$	Channel 1~4 LNA positive output
$PA_{1\sim4}N$	Channel 1~4 LNA negative output
$OUT_{1\sim4}P$	Positive polarity PGA output of channel 1~4
$OUT_{1\sim4}N$	Negative polarity PGA output of channel 1~4
PDC	PDC = 1, power down and enable external biasing, 450kΩ intermal pull down
EBC	External current biasing
GSC	Input of gain scaling control for all channels
A0, A1	Reserved, should connect to AV_{DD}
PG0, PG1	PGA Gain select inputs (PG0 = LSB, PG1 = MSB)
TGC	Attenuator control input
CM0~4	0.1µF bypass capacitors to ground

84-Lead BCC+ Package Outline (B2)

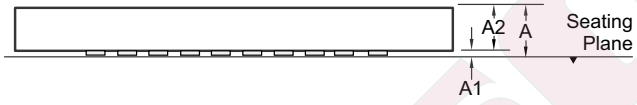
7.00x7.00mm body, 0.80mm height (max), 0.50mm pitch



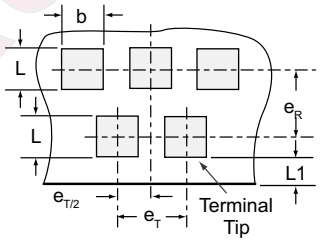
Top View



Bottom View



Side View



View A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D2	E	E2	e_R	e_T	L	L1
Dimension (mm)	MIN	0.65	0.05	0.60	0.20	6.85	4.55	6.85	4.55	0.50 BSC	0.50 BSC	0.20	0.10 REF
	NOM	-	-	0.65	0.30	7.00	4.70	7.00	4.70			0.30	
	MAX	0.80	0.10	0.70	0.40	7.15	4.85	7.15	4.85			0.40	

Drawings not to scale.

Supertex Doc. #: *DSPD-84BCC+B2 C101708.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com